University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

An Incomplete List of Topics Covered in this Course

Data Representation

Bits.

Unsigned, signed magnitude, 2's complement binary representation.

32-bit IEEE floating-point representation.

Hexadecimal notation.

ASCII representation.

Operations on Binary Data

1's complement operation.

Conversion to/from unsigned binary/2's complement/IEEE floating-point representation from/to decimal representation.

Modular arithmetics.

Addition and subtraction in unsigned binary and 2's complement representations.

Carry out and Overflow.

Boolean Algebra

Logic functions: NOT, OR, AND, XOR, XNOR, NOR, NAND.

Truth table.

Logical completeness.

Proof approaches: by construction, by induction.

Boolean algebra properties.

Boolean Algebra

Literals, implicants, prime implicants, duals, principle of duality.

Sum, product, minterm, maxterm, SOP, POS, canonical forms.

K-maps.

Don't cares.

Physical Layer

Transistors. MOSFETS.

CMOS.

Combinational Logic Circuits

2-level networks: AND-OR, OR-AND, NANO-NAND, NOR-NOR.

Design metrics: optimality, heuristics, constraints (area, speed, power).

Multiplexer, decoder.

Full adder, ripple-carry adder.

Comparator.

Bit-slicing.

Sequential Logic Circuits

R-S latch, S-R latch, gated D-latch.

Positive-edge triggered D flip-flop.

Register, shift register, resister with parallel load.

Active-low, active-high. Set, reset.

Clock, clock edge, clock gating.

Finite State Machine (FSM)

Clock synchronous sequential circuit.

Mealy and Moore models.

Synchronous counters, ripple counters.

Serialization.

FSM design: state and state representation, transition rules, list of abstract states, next-state table, state transition diagram.

Memory

Address space, addressability.

Abstract memory model.

RAM, ROM, SRAM, DRAM.

SRAM cell, DRAM cell.

SRAM slice.

Address selection. Coincident selection.

Building larger memories from smaller memories.

Von Neumann model

Model elements: processing unit, control unit, memory, input/output.

PC, IR, MAR, MDR.

Processor datapath, bus, control signals.

Instruction processing, instruction cycle.

Instruction Set Architecture (ISA), instruction encoding, instruction fields, opcodes.

LC-3 Computer Architecture

Datapath, control unit.

LC-3 instructions.

LC-3 binary coding.

LC-3 assembly language.

Assembly process.

Error Detection and Correction

Codewords, codes.

Bit error.

Odd/even parity.

Hamming distance.

Hamming code.

SEC-DEC.

C language and Programming Concepts

High-level language concepts: syntax, variables, operators, expressions, statements.

Functions in C: main, printf, scanf, …

Transforming tasks into program, flowchart.

Systematic Decomposition: sequential, conditional, and iterative constructs.

C statements: if, if-else, for, while.