University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

Static Hazards*

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Circuit Timing Can Cause Problems with Functionality

For our class, you need understand only the basics of timing:

- **how to estimate delay** (as gate delays),
- and **how to check for stable states** (trace changes until nothing changes).

In later classes, you will need to understand timing more deeply.

So let's take a look at how timing matters, just as a preview.

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Hazards, Glitches, and Errors

When a circuit **may have a problem** due to timing, we say that the circuit has a **hazard**.

If a combinational circuit's output is temporarily incorrect, we say that its output exhibits a **glitch**.

When a sequential circuit enters a state (a set of stored bits) that it should not enter by design, we say that the circuit has an **error**.

Typically, an error implies a glitch, which in turn implies a hazard, but not vice-versa.

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Static Hazards Allow for Change in Constant Output

The notes (Section 2.6.3* and following) discuss three types of hazards.

Static hazards

- allow a combinational circuit's output to change when moving between input combinations that should produce the same output.
- With a **static-1 hazard**, for example, both input combinations **should produce a constant output of 1**, but the **output may drop to 0** briefly because of timing.

Dynamic Hazards Allow Bouncing in Changing Output

Dynamic hazards

- occur when an input combination changes from one that should produce an output of 0 to a combination that should produce an output of 1 (or vice-versa).
- In these cases, the **output should change exactly once**.
- If a dynamic hazard is present, the **output may bounce between 0 and 1** before settling to its final value.

Essential Hazards Cannot be Eliminated

Essential hazards

- are **related to the function implemented** by the circuit.
- Unlike static and dynamic hazards, **they cannot be eliminated**.

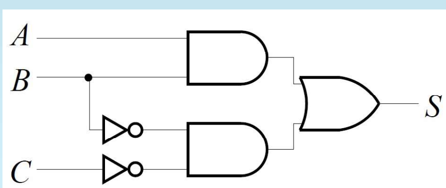
In clocked synchronous sequential circuits (and, thus, in the designs in our class), all essential hazards are mapped to **clock skew**.

Removing Static Hazards

If glitches in a circuit's output can cause problems, one can eliminate all static hazards.

Consider the circuit below. **What is S?**

S = AB + B'C'

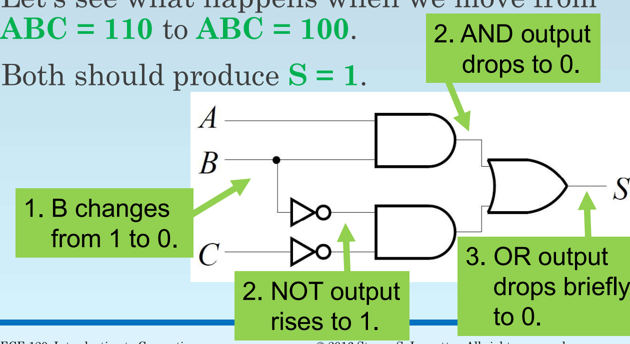


The Output S Should Stay at 1

So **S = AB + B'C'**.

Let's see what happens when we move from **ABC = 110** to **ABC = 100**.

Both should produce **S = 1**.



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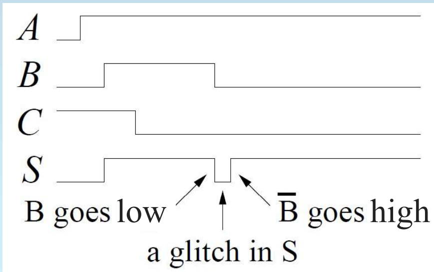
The Output S Drops to 0

The output glitches because the inverter for **B** delays the change in the lower AND gate.



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Fix Static Hazards by Adding More Gates

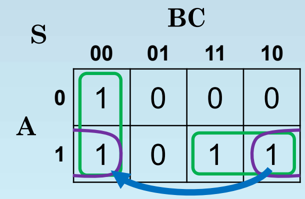
What can we do?

Take a look at the K-map.

The loops represent the AND gates.

ABC = 110 to **100** moves between loops.

Let's add a **new loop** (and a new AND gate).



The new AND gate will stay at 1.

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Read the Notes for More Information

See Notes Sections 2.6.3* through 2.6.6* if you want to learn more.